IN THE CLAIMS:

Please cancel claims 11-25 and amend the claims as follows:

1. (Currently Amended) A method for generating ~~a carry of~~ an effective address as a sum of a first and second numbers, the method comprising:

generating a first effective address based on an assumption there is a carry on a partial sum calculated from portions of the first and second numbers;

generating a second effective address based on an assumption there is no carry on the partial sum calculated from portions of the first and second numbers;

generating generate terms and propagate terms from the first and second numbers;

generating combined generate and propagate terms from the generate and propagate terms; ~~and~~

generating ~~the~~ at least a first carry term from the generate terms, the propagate terms, and the combined terms, wherein the first carry term indicates whether or not there is a carry on the partial sum; and

selecting one of the first second addresses based on the value of the first carry term.

2. (Currently Amended) The method of claim 1, wherein:

~~the step of generating combined terms comprises generating combined generate terms from the generate terms, and~~

the step of generating the first carry term comprises generating the carry from a limited subset of the generate terms, the propagate terms, and the combined generate terms.

3. (Original) The method of claim 2, wherein the step of generating combined generate terms from the generate terms comprises:

combining two of the generate terms to generate each of the combined generate terms.

4. (Currently Amended) The method of claim 3, wherein the step of generating at least the first carry term ~~combining two of the generate terms to generate each of the combined generate terms comprises~~:

generating at least the first carry term as a function of less than all possible combined generate terms ~~ORing the two generate terms to generate each of the combined generate terms~~.

5. (Currently Amended) The method of claim 1, wherein:

the first carry term is generated prior to or concurrently with the first and second effective addresses.

~~the step of generating combined terms comprises generating combined generate terms and combined propagate terms from the generate terms and propagate terms, respectively; and~~

~~the step of generating the carry comprises generating the carry from the generate terms, the propagate terms, the combined generate terms, and the combined propagate terms~~.

6. (Original) The method of claim 5 wherein the step of generating combined propagate terms from the propagate terms comprises:

combining two of the propagate terms to generate each of the combined propagate terms.

7. (Currently Amended) The method of claim 6 wherein the step of generating at least the first carry term ~~combining two of the propagate terms to generate each of the combined propagate terms~~ comprises:

generating at least the first carry term as a function of less than all possible combined propagate terms ~~ANDing the two propagate terms to generate each of the combined propagate terms~~.

8. (Currently Amended) An address ~~A carry~~ generation circuit for generating an effective address as ~~a carry of~~ a sum of a first and second numbers, ~~the carry generation circuit~~ comprising:

a plurality of inputs configured to receive the first and second numbers; ~~and~~

a fast carry ~~a generate and propagate term~~ generation circuit coupled to the inputs and configured to (a) generate propagate terms, generate terms, combined generate terms, and combined propagate terms from the first and second numbers, and (b) generate at least a first carry term from the propagate terms, the generate terms, the combined generate terms, and the combined propagate terms, wherein the first carry term indicates whether a partial sum of portions of the first and second numbers will generate a carry; and

an address selection circuit configured to select between a first effective address generated based on an assumption the partial sum will generate a carry and a second effective address generated based on an assumption the partial sum will not generate a carry.

9. (Currently Amended) The ~~carry~~ address generation circuit of claim 8 wherein the fast carry ~~generate and propagate term~~ generation circuit comprises:

a first circuit to generate the first carry term and a second circuit to generate a second carry term complementary to the first carry term ~~a plurality of first gates each of which configured to combine two of the generate terms to generate one of the combined generate terms~~.

10. (Currently Amended) The ~~carry~~ address generation circuit of claim 9 ~~8~~ wherein the address selection circuit ~~generate and propagate term~~ generation circuit comprises:

a first AND circuit controlled by the first carry term to select the first effective address and a second AND circuit controlled by the second carry term to select the second effective address ~~a plurality of second gates each of which configured~~

~~to combine two of the propagate terms to generate one of the combined propagate terms~~.

11-25. (Cancelled)

26. (Currently Amended) A method for generating a look-ahead carry of a sum of a first and second N-bit numbers, the method comprising:

adding, with an adder, M most significant bits of the first and second numbers assuming a carry-in from a partial sum of portions of the first and second numbers to generate a first sum output ~~the carry~~, M being at least one but less than N;

adding M most significant bits of the first and second numbers assuming no carry-in from the partial sum to generate a second sum output;

generating a look-ahead carry term based on lower significant bits of the first and second numbers; and

selecting one of the first and second sum outputs based on the value of the look-ahead carry term.

27. (Currently Amended) The method of claim 26 wherein the step of generating the look-ahead carry term ~~adding~~ comprises:

generating generate terms and propagate terms from portions of ~~the M most significant bits~~ of the first and second numbers;

generating combined generate terms and combined propagate terms from the generate terms and the propagate terms, respectively; and

generating the look-ahead carry term from the generate terms, the propagate terms, the combined generate terms, and the combined propagate terms.

28. (Currently Amended) The method of claim 27 wherein the step of generating the look-ahead carry term ~~propagate terms~~ comprises:

generating the look-ahead carry term prior to or concurrently with generating the first and second sum outputs ~~providing at least a first and second gates having a first dotted output; and~~

~~passing a first and second bits of the first and second numbers through the first and second gates, respectively, to the first dotted output so as to generate each of the propagate terms at the first dotted output.~~

29. (Currently Amended) The method of claim 28 wherein the step of generating the look-ahead carry term ~~generate terms~~ comprises:

generating a first look-ahead carry term and a second look-ahead carry term complementary to the first look-ahead carry term ~~providing M-1 combining gates having a second dotted output;~~

~~applying a third bit of the M most significant bits of the first number to all the M-1 combining gates and applying the remaining M-1 bits including a fourth bit to the M-1 combining gates one for one; and~~

~~passing the third bit and the fourth bit through a first combining gate of the M-1 combining gates to the second dotted output so as to generate each of the generate terms at the second dotted output.~~

30. (Currently Amended) ~~A carry generation~~ An adder circuit for generating ~~a carry of~~ a sum of a first and second N-bit numbers, ~~the carry generation circuit~~ comprising:

an addition circuit configured to receive M most significant bits of the first and second numbers and add the M most significant bits of the first and second numbers to generate, in parallel, a first sum assuming a carry-in resulting from a partial sum of a portion of the first and second numbers and a second sum assuming no carry-in resulting from the partial sum ~~the carry~~, M being at least one but less than N;

a fast carry generation circuit to generate at least a first carry term in conjunction with generating the first and second sums; and

a selection circuit to select one of the first and second sums based on the at least a first carry term.

31. (Currently Amended) The ~~carry generation~~ adder acircuit of claim 30 wherein the ~~addition~~ fast carry generation circuit is configured to:

generate terms and propagate terms from ~~the M most significant~~ bits of the first and second numbers;

generate combined generate terms and combined propagate terms from the generate terms and the propagate terms, respectively; and

generate the at least a first carry term from the generate terms, the propagate terms, the combined generate terms, and the combined propagate terms.

32. (Currently Amended) The carry generation circuit of claim 31 wherein the fast carry generation ~~addition~~ circuit is configured to generate the at least a first carry term based on a limited subset of the combined generate and propagate terms ~~comprises a propagate term generation circuit including at least a first and second gates having a first dotted output, the propagate term generation circuit being configured to pass a first and second bits of the first and second numbers through the first and second gates, respectively, to the first dotted output so as to generate each of the propagate terms at the first dotted output.~~

33. (Currently Amended) The carry generation circuit of claim 32 wherein:

the fast carry generation ~~addition~~ circuit is configured to generate the first carry term and a second carry term complementary to the first carry term; and

the selection circuit comprises a first AND circuit configured to select the first sum based on the first carry term and a second AND circuit configured to select the second sum based on the second carry term ~~further comprises a generate term generation circuit including M-1 combining gates having a second dotted output, the generate term generation circuit being configured to:~~

~~apply a third bit of the M most significant bits of the first number to all the M-1 combining gates and applying the remaining M-1 bits including a fourth bit to the M-1 combining gates one for one; and~~

~~pass the third bit and the fourth bit through a first combining gate of the M-1 combining gates to the second dotted output so as to generate each of the generate terms at the second dotted output.~~